REMARKS

Claims 1-17 and 19-26 are pending. Of those, claims 1, 14 and 20 are independent. By this reply, claim 18 has been canceled without prejudice to, or disclaimer of, subject matter contained therein.

Claim Objections

On page 2 of the Office Action, claims 2 and 10 are objected to because of typographical errors. By this reply, Applicant has clarified the typographical errors according to the Examiner's suggestions (for which Applicant is appreciative). Withdrawal of this objection is requested.

§112 Rejection

On page 3 of the Office Action, claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. By this reply, claim 18 has been canceled, making its rejection moot. Accordingly, withdrawal of the rejection is requested.

§102 Rejection

Beginning on page 4 of the Office Action, claims 1-4, 6, 12-15, 20-21, 23-24 and 26 are rejected under 35 U.S.C. 102(3) as being anticipated by U.S. Patent No. 6,532,519 to Arimilli et al. ('519).

The '519 patent is directed toward a technique for associating L3 cache memories with processors in a multi-processor system. Fig. 1 of the '519 patent depicts such a multi-processor system 10, which includes a plurality of central processor units (CPUs) 11a-11e, a system bus 20, a plurality of L3 caches 14a-14e and a corresponding plurality of cache controllers 19a-19e. Each of the cache controllers 19a-19e includes a mode register for determining which of the CPUs 11a-11e the corresponding L3 cache 14i should store data.

Different levels (and physical locations) of cache are denoted as "Li", e.g., L3. Each of the CPUs 11i includes an L1 cache 12i and an L2 cache

13i. As is well known, L1 cache is fabricated on the same chip as the CPU. Also well known is that L2 cache is often, but not always, fabricated on the same chip as the CPU. In the '519 patent, as L2 cache 13i is depicted within CPU unit 11i and in the same manner as L1 cache 12i, Applicant will assume for the sake of argument that both L1 cache 12i and L2 cache 13i are fabricated on the same chip as is CPU 11i.

As is also well known, L3 cache is not located on the same chip as the CPU, rather it is connected to a motherboard. In the '519 patent each L3 cache 14i connects via the corresponding cache controller 19i to system bus 20. Similarly, each CPU unit 11i connects to system bus 20.

Applicant acknowledges that the '519 patent discloses the use of a crossbar switch as an alternative implementation of system bus 20. Accordingly, Fig. 1 can be interpreted as depicting a crossbar switch 20 interposed between L3 cache 14i and CPU 11i. It would be unreasonable, however, to interpret crossbar switch 20 as being interposed between CPU 11i and either of L1 cache 12i or L2 cache 13i.

A distinction of amended claim 1 over the '519 patent is a crossbar interface between the processor and the on-chip cache (which is located on the same die as the processor). A distinction of independent claim 14 over the '519 patent is crossbar interface linking the on-chip caches, located on the same die as a plurality of processors, and the processors. A distinction of independent claim 20 over the '519 patent is providing a plurality of processors and a plurality of on-chip caches on the same die and then linking the processors and the caches using a crossbar interface. As noted above, crossbar switch 20 of the '519 patent interfaces between CPU 11i and only L3 cache 14i, where L3 cache 14i is not located on the same die as CPU 11i.

Claims 3-4, 6, 12-13, 15, 21, 23-24 and 26 depend at least indirectly from claims 1, 14 and 20, respectively, and distinguish over the '519 patent at least for the same reasoning.

In view of the foregoing discussion, §102(e) rejection of claims 1-4, 6, 12-15, 20-21, 23-24 and 26 over the '519 patent is improper and Applicant requests that it be withdrawn.

§103 Rejections

Beginning on page 7 of the Office Action, claims 5, 7-10, 16-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over '519 as applied to claims 1, 4, 14 and 20 above, and in view of U.S. Patent No. 5,737,757 to Hassoun et al. ('757).

The '757 patent has not been cited as teaching the distinction over the '519 patent, mentioned above. Accordingly, the distinction noted above also represents a distinction over the combination of the '519 patent modified according to the '757 patent. Claims 5, 7-10, 16-17 and 22 depend from claims 1, 14 and 20 at least indirectly, respectively, and accordingly distinguish over the combination of the '519 and '757 patents at least by dependency.

In view of the foregoing discussion the §103 rejection of claims 5, 7-10, 16-17 and 22 over the combination of the '519 and '757 patents is improper and Applicant requests that it be withdrawn.

Beginning on page 10 of the Office Action, claims 11 and 19 are rejected under §103(a) as being obvious over a combination of the '519 patent as modified according to the Handy reference (Fig. 2.4b and pages 44-46 of The Cache Memory Book, Jim Handy, 1998). Applicant traverses.

The Handy reference has not been cited as teaching the distinction over claims 1 and 14, noted above. Accordingly, that distinction of claims 1 and 14 also represent a distinction over the combination of the '519 patent as modified according to the Handy reference. Claims 11 and 19 depend from claims 1 and 14, respectively, and so distinguish over the combination of the '519 patent and the Handy reference at least by dependency.

In view of the foregoing discussion, the §103 rejection of claims 11 and 19 over the combination of the '519 patent and the Handy reference is improper and Applicant requests that it be withdrawn.

Beginning on page 11 of the Office Action, claim 25 is rejected under §103(a) as being unpatentable over the '519 patent taken alone. A distinction of claim 1 over the '519 patent has been noted above. Claim 11 depends from claim 1, and so distinguishes over the '519 patent at least by dependency. Accordingly, this rejection is improper and withdrawal is requested.

CONCLUSION

The issues in the case are considered to be resolved. Accordingly, Applicant again requests a Notice of Allowability.

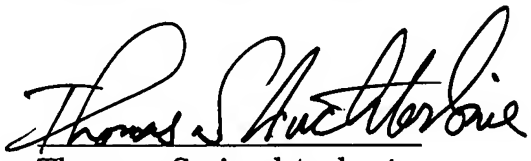
Person to Contact

In the event that any matters remain at issue in the application, the Examiners are invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

<remainder of page intentionally left blank>

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-2025 for any additional fees under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,
Donald C. SOLTIS, Jr.

By: 
Thomas S. Auchterlonie
Reg. No. 37,275

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 8910
Reston, VA 20195
(703) 668-8000

TSA/dg:tsa